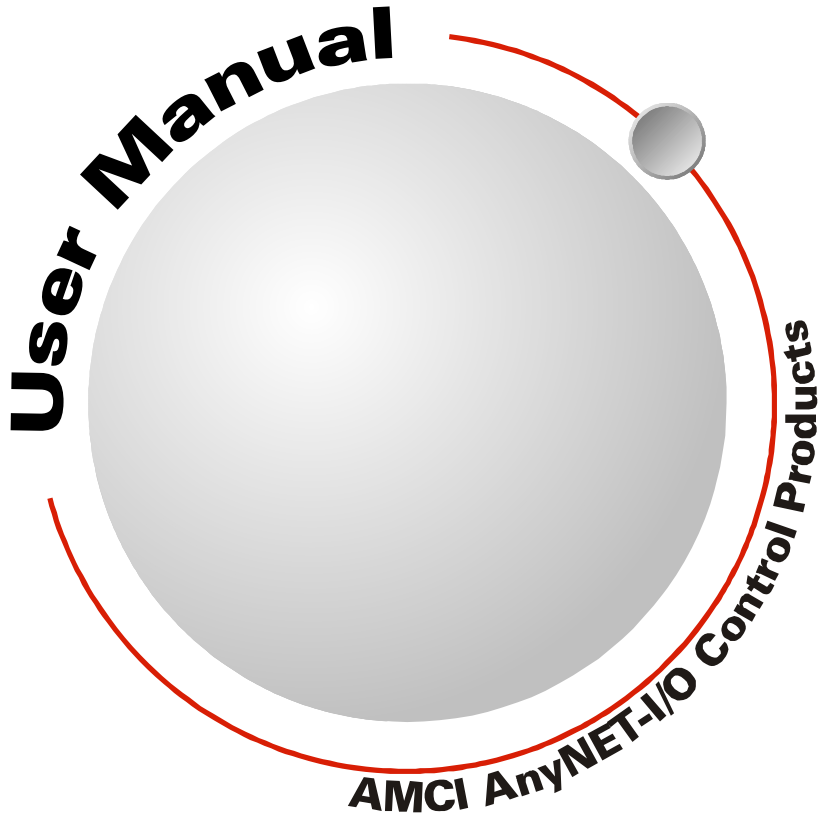
ADVANCED MICRO CONTROLS INC.

Manual #: 940-0A110

ANH2
AnyNET-I/O
2 Channel High Speed Counter & Encoder Module



GENERAL INFORMATION

Important User Information

The products and application data described in this manual are useful in a wide variety of different applications. Therefore, the user and others responsible for applying these products described herein are responsible for determining the acceptability for each application. While efforts have been made to provide accurate information within this manual, AMCI assumes no responsibility for the application or the completeness of the information contained herein.

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All equipment being returned to AMCI for repair or replacement, regardless of warranty status, must have a Return Merchandise Authorization number issued by AMCI. Call (860) 585-1254 with the model number and serial number (if applicable) along with a description of the problem during regular business hours, Monday through Friday, 8AM - 5PM Eastern. An "RMA" number will be issued. Equipment must be shipped to AMCI with transportation charges prepaid. Title and risk of loss or damage remains with the customer until shipment is received by AMCI.

24 Hour Technical Support Number

24 Hour technical support is available on this product. If you have internet access, start at www.amci.com. Product documentation and FAQ’s are available on the site that answer most common questions.

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We Want Your Feedback

Manuals at AMCI are constantly evolving entities. Your questions and comments on this manual are both welcomed and necessary if this manual is to be improved. Please direct all comments to: Technical Documentation, AMCI, 20 Gear Drive, Terryville CT 06786, or fax us at (860) 584-1973. You can also e-mail your questions and comments to *techsupport@amci.com*

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About This Manual

Read this chapter to learn how to navigate through this manual and familiarize yourself with the conventions used in it. The last section of this chapter highlights the manual's remaining chapters and their target audience.

Audience

This manual explains the installation and operation of the ANH2 Two Channel High Speed Counter / Encoder Module from AMCI. It is written for the engineer responsible for incorporating the ANH2 into a design as well as the engineer or technician responsible for its actual installation. If there are any unanswered questions after reading this manual, call the factory. An applications engineer will be available to assist you.

Applicable Units

This manual applies to all ANH2 modules, including those that have an integral network connection. If your ANH2 module has a network interface, such as the ANH2E, you will have to refer to the appropriate AnyNET-I/O Network Interface manual for information on connecting the module to your network. These manuals can be found in the PDF document section of our website at ***www.amci.com/documents.asp***.

NOTE The AnyNET-I/O product line is constantly evolving. Check our website, ***www.amci.com*** for the latest information on available modules and network interfaces in the AnyNET-I/O line.

Trademark Notices

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Revision Record

This manual, 940-0A110, is the first release of this manual. It was released on August 7thth, 2015.

Navigating this Manual

This manual is designed to be used in both printed and on-line forms. Every chapter is an even number of pages, making it easy to print individual chapters on a duplex, or double sided, printer. The manuals' on-line form is a PDF document, which requires Adobe Acrobat Reader version 6.0+ to open it. Please note that the PDF document was created with version 9 of Adobe Acrobat. When you open this file with Acrobat Reader versions 6 through 8, you may see a warning message stating that the file was created with a later version of Acrobat. This warning can be safely ignored as this file has been tested with these versions of Acrobat Reader.

Bookmarks of all the chapter names, section headings, and sub-headings are in the PDF file to help you navigate through it. The bookmarks should have appeared when you opened the file. If they didn't, press the F5 key on Windows platforms to bring them up.

Throughout this manual you will also find ***blue text that functions as a hyperlink*** in HTML documents. Clicking on the text will immediately jump you to the referenced section of the manual. If you are reading a printed manual, most links include page numbers.

The PDF file is password protected to prevent changes to the document. You are allowed to select and copy sections for use in other documents and, if you own Adobe Acrobat version 6.0 or later, you are allowed to add notes and annotations.

Manual Conventions

Three icons are used to highlight important information in the manual:

NOTE NOTES highlight important concepts, decisions you must make, or the implications of those decisions.

CAUTION CAUTIONS tell you when equipment may be damaged if the procedure is not followed properly.

WARNING WARNINGS tell you when people may be hurt or equipment may be damaged if the procedure is not followed properly.

The following table shows the text formatting conventions:

Format	Description
Normal Font	Font used throughout this manual.
Emphasis Font	Font used the first time a new term is introduced.
Cross Reference	When viewing the PDF version of the manual, clicking on the cross reference text jumps you to referenced section.

Where To Go From Here

This manual contains information that is of interest to everyone from engineers to operators. The table below gives a brief description of each chapter's contents to help you find the information you need to do your job.

CHP Num.	Chapter Title	Chapter Description
1	***Introduction to the ANH2***	Intended for anyone new to the ANH2, this chapter gives a complete overview of the unit.
2	***Installing the ANH2***	Information on physically installing the ANH2 in your system. Network configuration is covered is a separate manual.
3	***Network Output Data Format***	This chapter explains how to configure the ANH2 for your application using data written from your host controller.
4	***Network Input Data Format***	This chapter explains the format of the counter and limit switch data returned to the host controller from the ANH2.
5	***Error Codes***	This chapter lists the available error codes from the ANH2 as well as the errors that cause them.
6	***Default Parameter Values***	This chapter lists the default values for all parameters available on the ANH2.

CHAPTER 1

INTRODUCTION TO THE ANH2

This manual is designed to get you quickly up and running with the ANH2 High Speed Counter / Encoder Module. It is possible to purchase this module with or without a network interface. This manual only covers the functionality unique to the ANH2. Information on connecting to the network interface is available in the appropriate AnyNET-I/O Network Interface manual available on the AMCI website.

AnyNET-I/O

The ANH2 is an expansion to the AnyNET-I/O product line from AMCI. The concept of this product line is simple: specialty and/or high speed I/O that can be attached to any popular industrial network; hence the name *AnyNET-I/O*.

AnyNET-I/O is designed for a broad range of applications, from small machines with a single control enclosure, to large machines that use distributed I/O extensively to minimize wiring costs.

What makes the AnyNET-I/O line different is that modules are available with or without a network interface. Eliminating the need for a separate networking module lowers the total cost of ownership for all applications, but especially for the cost sensitive small machines that only require one or two sophisticated functions.

Like many modern controllers, AnyNET-I/O modules are designed to be DIN rail mounted. Up to six AnyNET-I/O modules can be stacked together and accessed over a single network interface. "Stacking" is accomplished through a small backplane connector that snaps into the DIN rail before the AnyNET-I/O modules are installed. These connectors allow the AnyNET-I/O modules to communicate with each other. To the network, the stack of modules appear as one continuous block of I/O words. The logical position within the stack is determined by a DIP switch setting on the front of the module.

Figure 1.1 AnyNET-I/O Module Stack

Module Overview

The ANH2 is the first high speed counter / encoder module for the AnyNET-I/O product line. The module offers two counter channels.

Two Independent Counters

Each counter has three differential, 5 to 24 Vdc inputs. ±A, ±B, ±Z.

Counter Modes:

- Pulse Count on A with external direction control on B.
  Increment when B is inactive, decrement when B is active.
- Pulse Count on A with internal direction control on network data bit.
  Increment when data bit equals "0", decrement when data bit equals "1".
- Up/Down pulse counter.
  Increment on A, Decrement on B.
- Quadrature Encoder on A and B. (1X, 2X, or 4X decoding)

Module Overview (continued)

Two Independent Counters (continued)

Capture and Gate Modes: (Z input used for external control.)

- Capture/Continue: Capture count value on positive transition of Z.
- Capture/Preset/Continue: Capture count value and preset count on positive transition of Z.
- Capture/Hold/Resume: Capture count value on positive transition of Z, ignore pulse inputs while Z is active.
- Capture/Preset/Hold/Resume: Capture count value on positive transition of Z, preset position value and ignore pulse inputs while Z is active.

Each counter can be configured as a linear or ring counter.

- Programmable min/max counts
- Linear Counters count between the min/max counts and sets an overflow or underflow bit when outside the range.
- Ring counters count between the min/max values and automatically rolls over to other value if the counter overflows/underflows.

4 MHz counting rate. (2 MHz input when using 2X decode with encoder, 1 MHz input with 4X decode)

- Rate reported with a resolution of one count.
- Programmable min/max rate limits. The ANH2 sets rate overflow/underflow bits if the count rate is outside of these limits.

±2,147,483,647 count range (signed 32 bit value)

- Network data bit can be used to preset counter value in all of the capture and gating modes.

Outputs

4 physical DC outputs are available.

- 5 -30Vdc, Sourcing
- 1 amp max. per output
- 2 amp max. per module
- Output are protected with a PTC resettable fuse.

4 Virtual Outputs are available as network data only

Outputs controlled by limit switch setpoint pairs, Force ON bits, and Force OFF bits.

16 Limit Switch Setpoint Pairs

Count or Rate based limits.

- Normal Limits: Position/Rate ON → Position/Rate OFF
  - If ON point is less than OFF point, output is *active* when ON point <= count/rate <= OFF point.
  - If ON point is greater than OFF point, output is *inactive* when ON point <= count/rate <= OFF point.
- Timed Limits: Position/Rate ON → Time OFF
  - Time is programmed in milliseconds, range of 1 to 32,767.
  - Output becomes active when ON point = count/rate. Output turns off after programmed time.
  - ON point is not direction sensitive. Output will trigger if count/rate is increasing or decreasing when it passes through the ON point.
  - Once triggered, the count/rate value is ignored until the timer times out. If the “ON point = count/rate” condition again occurs while the output is triggered, the “ON point = count/rate” condition is ignored.

Module Overview (continued)

16 Limit Switch Setpoint Pairs (continued)

Programmable allocation to either counter. Number of limits assigned to counter 1 is programmed as "n". Limits 1 to "n" are assigned to counter 1, Limits "n+1" to 16 are assigned to counter 2. "n" can equal 0 or 16, assigning all setpoints to counter 2 or counter 1 respectively.

Each limit switch has a separate enable/disable bit.

Limit switches can be assigned to any/all outputs. The state of each output is the logical OR of the values of all of the limit switches assigned to the output.

- The most common use of this setup allows the ANH2 to have multiple setpoint pairs per output.
- This setup also allows an output state controlled by both counters. For example, an output can be programmed to change state if the rate output from either of the two counters falls outside of a programmed range. (Speed tracking)

The output range includes the "OFF" setpoint. For example, a setpoint pair of 45/215 turns on at 45 and is on through (and including) 215. AMCI Programmable Limit Switch modules would turn on at 45 and off at 215. This change allows the ANH2 to offer single ended outputs on linear counters by setting the appropriate setpoint to the minimum or maximum counter value. For example, program a linear counter to a range of ±1,000 counts. Programming a setpoint pair from 0 to 1,000 would have the output on for all positive counter values, including when the counter overflows.

Output Force

Allows the user to force an output on or off regardless of the state of any limits switches assigned to it.

- Allows the outputs to be used as general purpose outputs
- Force ON takes precedence over limit switch state(s)
- Force OFF takes precedence over Force ON and limit switch output state(s).

Module Connectors

The ANH2 has two connectors. The power connector is located on the bottom of the module. The I/O connector is located on the top. If the ANH2 has a network connection, the network connector will be located on the bottom of the module.

Power Connector

The figure below shows the location of the power connector as well as the location of the network connector if it is available on the module.

The ANH2 requires a 10 to 28 Vdc supply to power the module. Surges to 30 Vdc will not damage it.

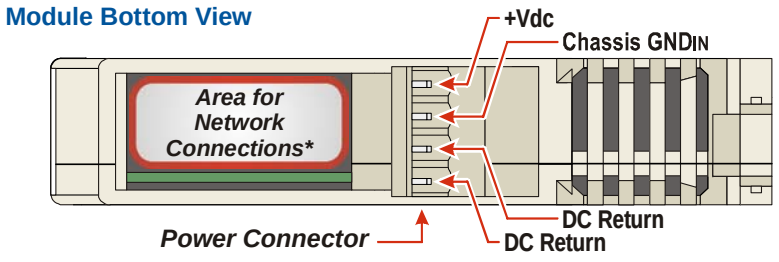


Figure 1.2 Power Connector Location

The mating connector is included with the ANH2. Spares are available from AMCI under the part number MS-4M.

Module Connectors (continued)

I/O Connector

Figure 1.3 below shows the pin out of the I/O connector on the ANH2 module. All mating connectors are included with the module. Additional connectors can be order for AMCI under the part number MS-2x11.

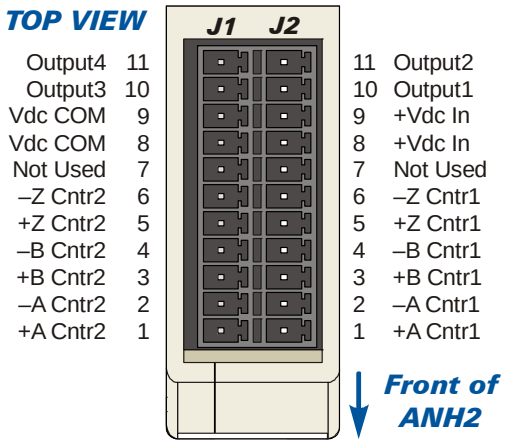


Figure 1.3 I/O Connector Pin Out

- +Vdc In and Vdc COM pins are used to power the outputs. Note that you can use the same supply to power the inputs. You can jumper from the power pins to the appropriate side of the input if you are using them as single ended inputs instead of differential inputs.
- The same power supply can be used to power the module and the I/O. Connections must be made at the power connector and the I/O connector. The two sections of the module are isolated.

Front Panel Status LED

The ANH2 has a single bi-color red/green status LED on the front of the module.

- **Steady Green:** Module OK.
- **Steady Red:** Communications failure. An ANH2 with a network interface is receiving data on the interface, but its AnyNET-I/O stack address is not equal to zero.

The LED will flash red/green while the module initializes during power up.

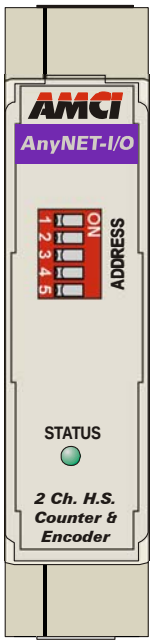


Figure 1.4 Status LED

Specifications

Number of Counters

Two

Number of Inputs Per Counter

Three (±A, ±B, ±Z)
- Differential
- ON Voltage Range: 5 Vdc to 24 Vdc
- OFF Voltage Range: 0 Vdc to 2 Vdc
- Maximum Input Current: 7.5mA @ 24Vdc

Counting Modes

Four
- Count on A, Direction Control on B
- Count on A, Direction Control on internal bit
- Increment on A, Decrement on B
- Quadrature Encoder on A, B
  (X1, X2, or X4 decoding supported)

Capture and Gate Modes

Four. (Capture/Gate uses Z input)
- Capture/Continue
- Capture/Preset/Continue
- Capture/Hold/Resume
- Capture/Preset/Hold/Resume

Counter Preset

Can be preset with a positive transition on the Z input or with network data from the host.

Limit Switch Setpoints Pairs

Sixteen total, shared between the two counters.

Count or Rate based limits
- Position ON / Position OFF
- Rate ON / Rate OFF
- Position ON / Time OFF
- Rate ON / Time OFF

Timer range: 1 to 32,767 milliseconds

Number of I/O Words per Module

20 Input Words, 20 Output Words

Programming Storage

FLASH Memory.

Outputs

Eight Total. Four Real, Four Virtual

Real Outputs are connected to DC sourcing drivers on the ANH2 and are also reported to the host controller.

Virtual Outputs are only reported to the host controller

Outputs are controlled by the state of the limit switches assigned to them as well as Force ON / Force OFF bits that are available in the network data from the host controller.

Output Driver

Voltage Range: 12 Vdc to 24 Vdc

Maximum Output Current:
1 Adc per output, 2 Adc per module

Fuse: PTC resettable
Will carry 3 Adc @ 20°C.
Guaranteed trip at 6 Adc

An external supply is required for operation.

Power Supply

10 to 28 Vdc, surge to 30 Vdc without damage to module.

ANH2: 120 mA @ 24 Vdc (2.9W)

I/O power requirements must be considered when sizing the supply.

Environmental Conditions

Operating Temperature:-4 to 122 °F
(-20 to 50 °C)

Relative Humidity:5 to 95%
(w/o condensation)

Storage Temperature:-40 to 185 °F
(-40 to 85 °C)

Connectors

Mating connectors are included with the ANH2. They are also available these AMCI numbers.

Connector	AMCI Part #	Wire	Strip Length	Min. Tightening Torque
I/O	MS-2X11	28 - 16 AWG	0.275 inches	Spring Cage Connector
Power	MS-4M	28 - 12 AWG	0.394 inches	4.43lb-in (0.5 Nm)
Backplane	IC-5	Not Applicable		

Notes

CHAPTER 2
INSTALLING THE ANH2

This chapter contains information on properly handling the ANH2 as well as mounting the module in a safe environment. This chapter also covers how to wire your field I/O to the ANH2.

Module Installation

Module Location

AnyNET-I/O modules are suitable for use in industrial environments that meet the following criteria:

- Only non-conductive pollutants normally exist in the environment, but an occasional temporary conductivity caused by condensation is expected.
- Transient voltages are controlled and do not exceed the impulse voltage capability of the product's insulation.

Note that these criteria apply to the system as a whole. These criteria are equivalent to the *Pollution Degree 2* and *Over Voltage Category II* designations of the International Electrotechnical Commission (IEC).

Safe Handling Guidelines

Prevent Electrostatic Damage

CAUTION Electrostatic discharge can damage an AnyNET-I/O module if you touch the rear bus connector pins. Follow these guidelines when handling the module.

1) Touch a grounded object to discharge static potential before handling the module.
2) Work in a static-safe environment whenever possible.
3) Wear an approved wrist-strap grounding device.
4) Do not touch the pins of the bus connector or I/O connector.
5) Do not disassemble the module
6) Store the module in its anti-static bag and shipping box when it is not in use.

Prevent Debris From Entering the Module

WARNING During DIN rail mounting of all devices, be sure that all debris (metal chips, wire strands, tapping liquids, etc.) is prevented from falling into the module. Debris may cause damage to the module or unintended machine operation with possible personal injury. The DIN rail for the modules should be securely installed and grounded before the modules are mounted on it.

Remove Power Before Servicing in a Hazardous Environment

WARNING Remove power before removing or installing any modules in a hazardous environment.

Module Installation (continued)

Module Mounting

Dimensions

The figure below shows the dimensions of the ANH2 AnyNET-I/O module. These modules are low power modules that do not require any additional spacing when mounting them. Refer to the installation instructions of the appropriate AnyNET-I/O network interface module for complete information on spacing needed to install the module.

NOTE You may need to ground the sensor cable shields at the module. There is an earth ground pin on the power connector, but if you have multiple shields, it will be better to ground them to the DIN rail. If you decide to do this, make sure your DIN rail is long enough to mount the AnyNET-I/O modules and ground the cable shields.

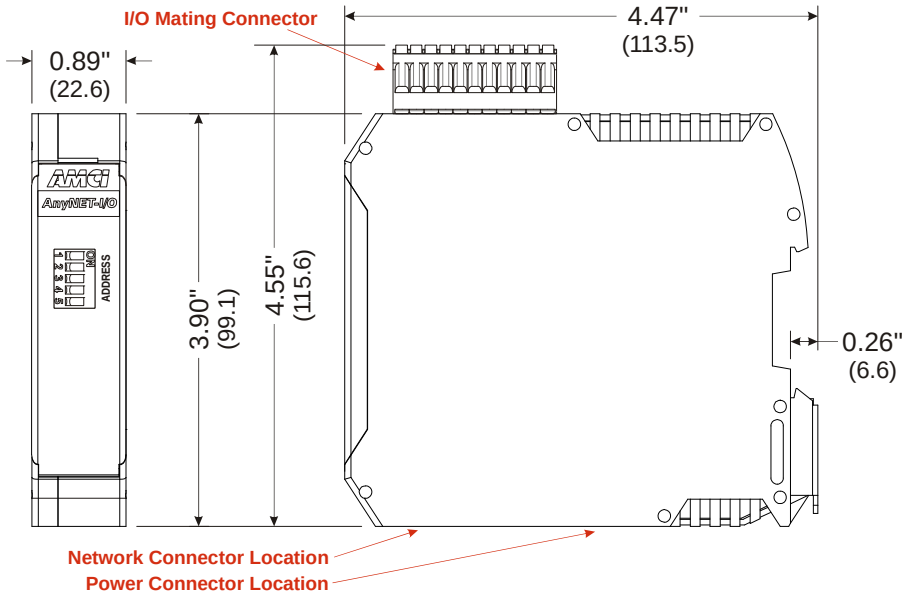


Figure 2.1 ANH2 Outline Drawing

Module Installation (continued)

Module Mounting (continued)

Compatible DIN Rail

The ANH2 can be mounted on following DIN rail:

- EN 05 022 - 35 x 7.5 (35 x 7.5 mm)

If you are only installing one ANH2 module instead of an interconnected stack, then you can also use the following DIN rail:

- EN 05 022 - 35 x 15 (35 x 15 mm)

NOTE The EN 05 022 - 35 x 15 DIN rail is unacceptable when installing multiple AnyNET-I/O modules as a stack. The IC-5 connector that is used to interconnect the modules requires the EN 05 022 - 35 x 7.5 DIN rail for proper operation.

The DIN Rail must be securely mounted to a panel and solidly grounded before the module is installed. Grounding is usually accomplished through the mounting hardware, by first removing any paint or other material from all surfaces that may interfere with proper grounding. Another option is to install a heavy gauge wire from the DIN rail to your system's ground bus.

Installing IC-5 Connectors

IC-5 connectors must be used when more than one module is installed as an interconnected stack. The ANH2 uses one IC-5 connector. Figure 2.2 shows how to install the IC-5 connectors in the DIN rail.

NOTE

1) EN 05 022 - 35 x 7.5 DIN rail must be used. The IC-5 connectors are not properly supported in EN 05 022 - 35 x 15 DIN rail
2) Note the orientation of the IC-5 connectors when installing them. The module key goes towards the bottom of the DIN rail.

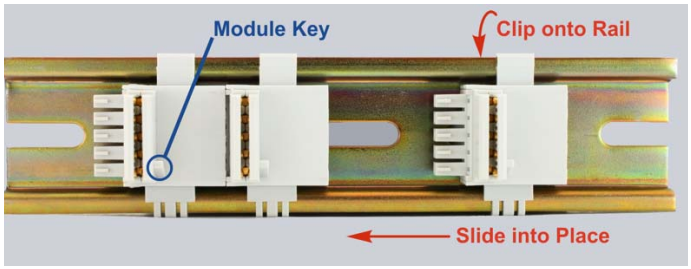


Figure 2.2 IC-5 Connector Installation

Mounting the AnyNET-I/O Module

Mounting an AnyNET-I/O module is a very simple process thanks to the design of the enclosure.

1) Partially engage the connector into the enclosure.
2) Engage the top clip in the enclosure with the top of the DIN rail and rotate the module down until the metal bracket snaps on to the DIN Rail.

Once all of your modules are installed, it is strongly suggested to use the end caps from Phoenix Contact with the part number of 271 37 80 to secure the modules on the DIN Rail. These end caps prevent the module from sliding along the DIN rail if it is subjected to shock or vibration during machine operation.

Module Installation (continued)

Stack Addressing

Each module is a stack needs to be given an address before the system will operate correctly. The address is set with the five position DIP switch on the front of the module.

NOTE

1) The module with the network interface for the stack must have all of its DIP switches off. (This is called address 0.) This is the only module in the stack that can have a direct network connection.
2) Only a single switch should be in the "ON" position when setting the address.
3) If a module has a network interface, this interface is disabled if the module has a non-zero address. This allows two modules with network interfaces to work in a single stack.

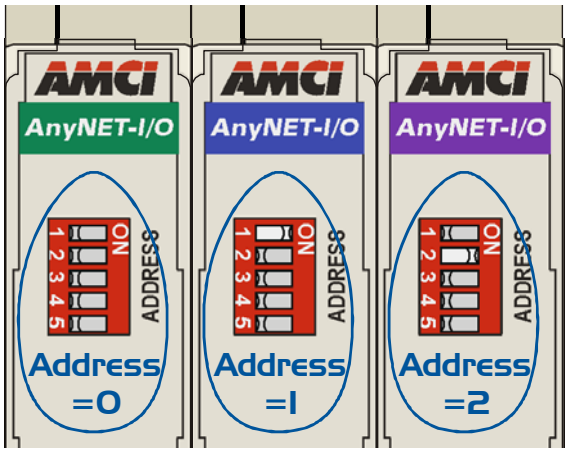


Figure 2.3 Addressing Example

Figure 2.3 is a close up of three modules in an AnyNET-I/O Stack. The module on the left is an unit with a network interface, and has an address of zero (All DIP switches off.) This module has the active network interface and connects the stack to the network. Reading left to right, the remaining modules have addresses of one and two respectively. These modules can be any type of AnyNET-I/O modules. If they have network interfaces, these interfaces are disabled.

Powering the Module

Required Power

The ANH2 requires a 10 to 28 Vdc supply to power the module. Surges to 30 Vdc will not damage it. Current draw is 120 mA @ 24 Vdc (2.9W).

This current draw does not include current through the inputs or outputs. If using the same supply to power the I/O, their load must be considered when sizing the supply.

- Inputs require a maximum of 7.5 mA each.
- Outputs can source up to 1 Adc each, with a module limit of 2 Adc.

Powering the Module (continued)

Wiring

As shown in the figure below, the power connector is located on the bottom of the module. The mating connector is included with the ANH2. Spares are available from AMCI under the part number MS-4M. They are also available from Phoenix Contact under their part number 187 80 37.

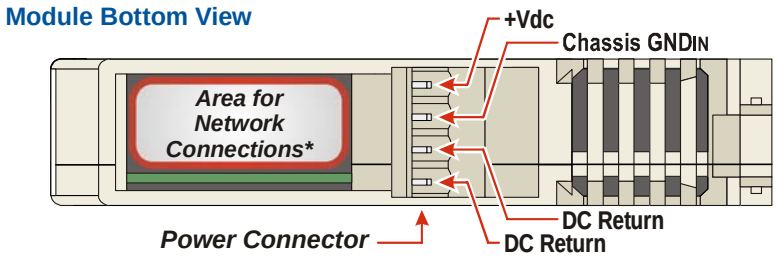


Figure 2.4 Power Connector Location

Power connections should be tight, as loose connections may lead to arcing which will heat the connector. Phoenix Contact specifies a tightening torque of 4.4 to 5.4 lb-in (0.5 to 0.6 Nm).

The power supply is connected to the pins marked "+Vdc In" and "DC Return". The "Chassis GND" pin is used to attach the ANH2 to earth ground.

NOTE

1) AnyNET-I/O modules are electrically isolated from the DIN rail by their mounting, but the Chassis GND connection is common to all of the modules in the stack through a pin of the IC-5 connector. At least one module in the AnyNET-I/O Stack must be attached to earth ground through a heavy gauge stranded wire to ensure reliable operation of the stack.
2) Each ANH2 module must have its own power connection.
3) AnyNET-I/O modules will not be damaged if it is plugged into the InterConnect bus while power is applied, but the stack will not reconfigure itself to accept the new module.

I/O Connector Pin Out

Figure 2.5 below shows the pin out of the I/O connector on the ANH2 module. All mating connectors are included with the module. Additional connectors can be order for AMCI under the part number MS-2x11.

- +Vdc In and Vdc COM pins are used to power the outputs. Note that you can use the same supply to power the inputs. You can jumper from the power pins to the appropriate side of the input if you are using them as single ended inputs instead of differential inputs.
- The same power supply can be used to power the module and the I/O. Connections must be made at the power connector and the I/O connector. The two sections of the module are isolated.

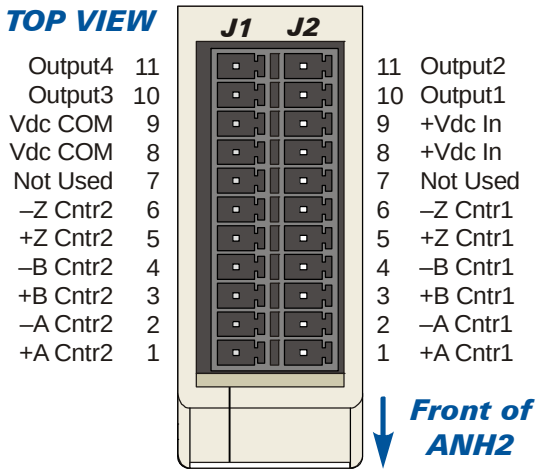


Figure 2.5 I/O Connector Pin Out

Sensor Input Wiring

Input Specifications

The ANH2 has three differential inputs per channel. They accept 5 to 27Vdc without the need for an external current limiting resistor.

Because they are low power signals, cabling from the sensor to the ANH2 should be done using a twisted pair cable with an overall shield. The shield should be grounded at the end when the signal is generated, which is the sensor end. If this is not practical, the shield should be grounded to the same ground bus as the ANH2.

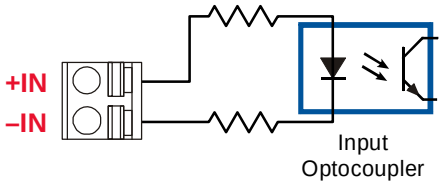
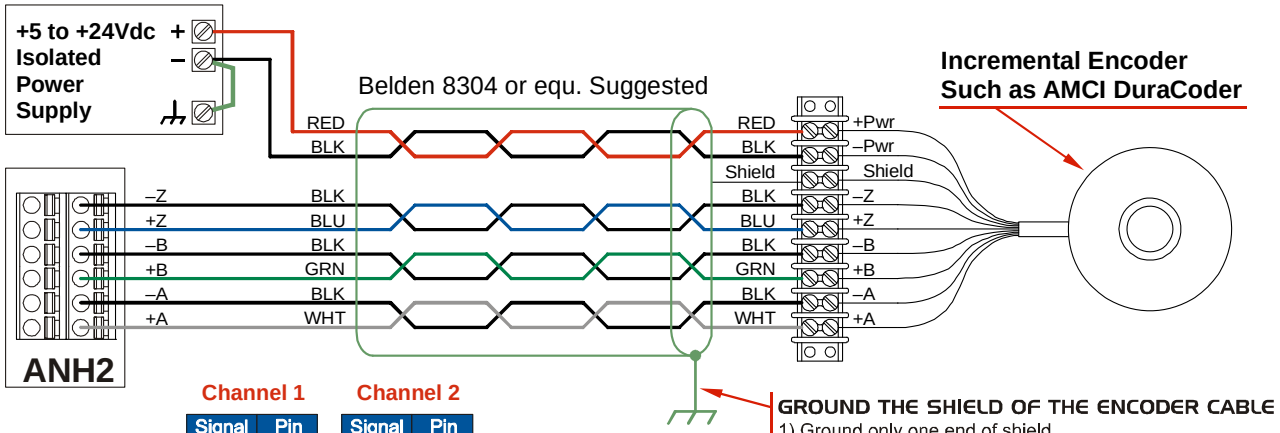


Figure 2.6 Input Schematic

Differential Sensors

The sensor inputs on the ANH2 accept 5 to 24Vdc differential signals. An incremental encoder is used in the figure below as an example of how to wire differential inputs. Discrete sensors with differential outputs are wired in the same way.



Channel 1

Signal	Pin
+A1	J2-1
–A1	J2-2
+B1	J2-3
–B1	J2-4
+Z1	J2-5
–Z1	J2-6

Channel 2

Signal	Pin
+A2	J1-1
–A2	J1-2
+B2	J1-3
–B2	J1-4
+Z2	J1-5
–Z2	J1-6

Figure 2.7 Differential Input Wiring

Sensor Input Wiring (continued)

Single Ended Wiring

Figures 2.8 and 2.9 below shows how to wire the sensor inputs to sourcing or sinking sensors. Incremental encoders with single ended outputs are wired in the same way.

Sourcing Sensor

Channel 1		Channel 2	
Signal	Pin	Signal	Pin
+A1	J2-1	+A2	J1-1
–A1	J2-2	–A2	J1-2
+B1	J2-3	+B2	J1-3
–B1	J2-4	–B2	J1-4
+Z1	J2-5	+Z2	J1-5
–Z1	J2-6	–Z2	J1-6

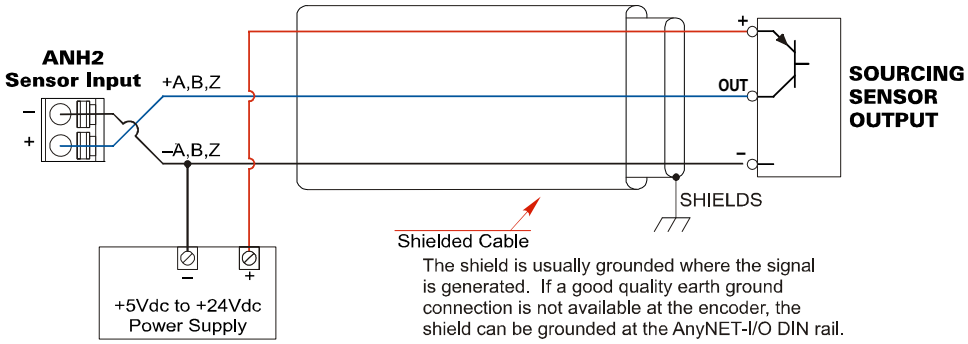


Figure 2.8 Sourcing Sensor Wiring

Sinking Sensor

Channel 1		Channel 2	
Signal	Pin	Signal	Pin
+A1	J2-1	+A2	J1-1
–A1	J2-2	–A2	J1-2
+B1	J2-3	+B2	J1-3
–B1	J2-4	–B2	J1-4
+Z1	J2-5	+Z2	J1-5
–Z1	J2-6	–Z2	J1-6

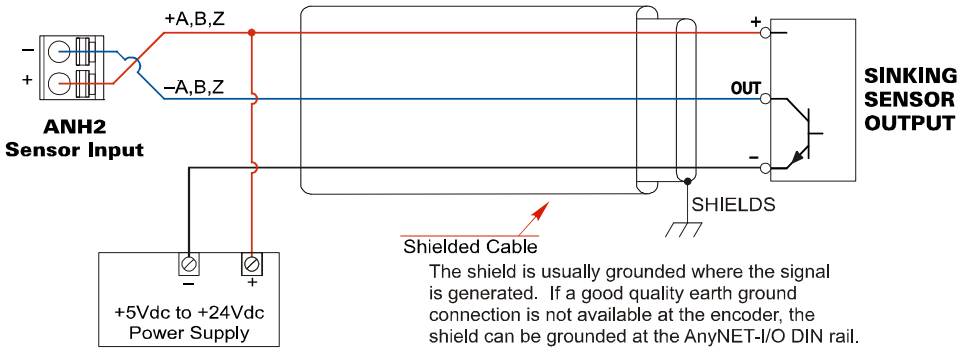
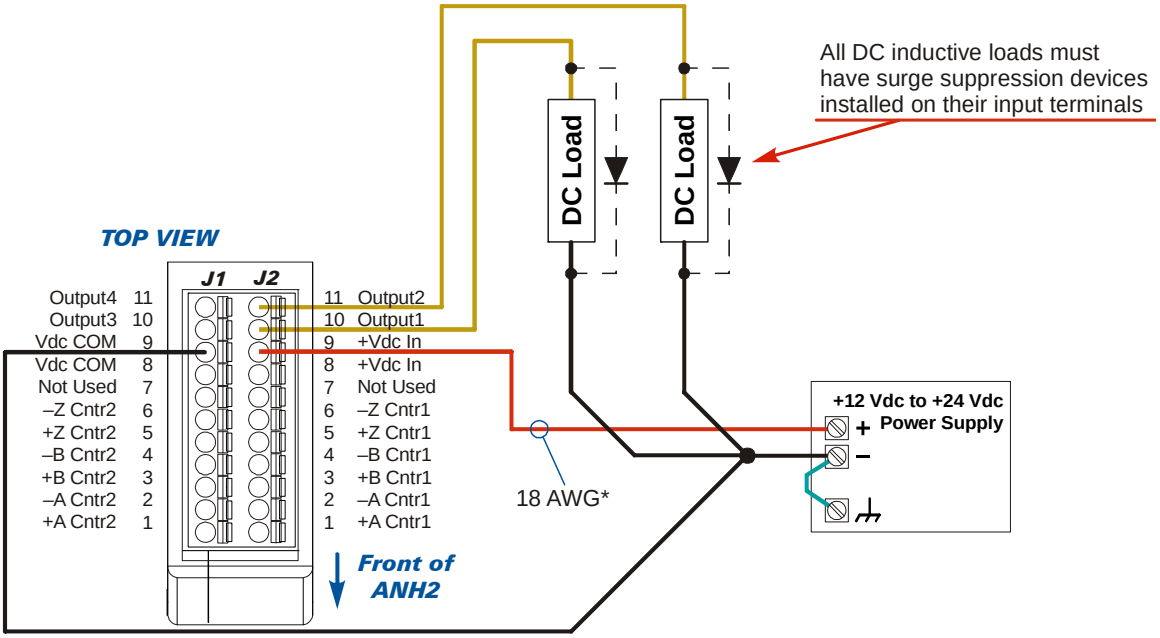


Figure 2.9 Sinking Sensor Wiring

Digital Output Wiring

The ANH2 has four outputs available on the I/O connector. These are 12 to 24Vdc sourcing outputs. All four outputs share the single power supply, which must be connected to either or both of the "+Vdc In" pins shown in figure 2.10 below. Connections to outputs 1 and 2 are shown in the diagram. Outputs 3 and 4 are wired in the same way.



* Power supply wiring should be made with 18 AWG wire.
The ANH2 can conduct 3 to 6 Adc during a fault condition.

Figure 2.10 ANS1 Output Wiring

NOTE

1) The "+Vdc In" pins carry the current for all of the outputs. The connector is rated for a maximum of eight amps per pin.

2) Overloading any of the outputs will trip the internal resettable fuse, which will temporarily disable all four outputs. The fuse will carry 3 Adc @ 20°C and is guaranteed to trip at 6 Adc regardless of the ambient temperature. 18 AWG wire should be used when wiring power to the AH2.

3) A connection between the power supply common and one or both of the "Vdc COM" pins in the ANH2 is required to enable the protection circuitry on the ANH2.

4) All inductive loads must have surge suppression devices installed on their input terminals. Repeated high voltage spikes on the outputs of the ANH2 may permanently damage them. This protection is required in addition to the protection circuitry on the ANH2.

Multi-Word Parameters

Most of the values used to program the ANH2, as well as values reported back to the host controller, can exceed ±32,768 counts. Therefore, they require two words of storage and they are transmitted as 32 bit values. The least significant word (LSW) contains the lower sixteen bits of the value and the most significant word (MSW) contains the remaining bits. When determining the values needed when programming the ANH2, it is easiest to convert the parameter value to hexadecimal and enter these values into your data table. Many host controllers display 16 bit values in 2's-compliment notation. Sixteen bit values between 32,768 and 65,535 will appear as negative numbers when viewed as decimals.

Value (dec)	Value (hex)	MSW (hex)	MSW (dec)	LSW (hex)	LSW (dec)
50,800	16#0000:C670	16#0000	0	16#C670	-14,736
16,702,650	16#00FE:DCBA	16#00FE	254	16#DCBA	-9030
-16,702,650	16#FF01:2346	16#FF01	-255	16#2346	9,030
-1234	16#FFFF:FB2E	16#FFFF	-1	16#FB2E	-1234

Table 3.1 Multi-word Data Format

Depending on the host controller, it may be possible to directly copy 32 bit integer values directly into the two 16 bit registers used by the ANH2 module.

Transmit Bit

The Transmit Bit is used to tell the ANH2 when a new command is being written to it. Bit 15 of the Command Word in the Network Output Data (Output Word 0, bit 15) is always the Transmit Bit.

The ANH2 only accepts commands when the Transmit bit makes a 0→1 transition. Therefore, this bit must be reset between commands. The easiest way to do this is to write a value of zero into the Command Word before writing the next command. Once this bit is reset, the ANH2 will respond by resetting the Acknowledge Bit. At this point, another command can be written to the ANH2.

Counter Configuration Programming Block

Word Numbers	Word Number 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**Program Control Word**															
	TRMT	Echo	0	0	0	0	Pgm2	Pgm1	0	0	0	0	0	0	0	1
1	0	0	0	0	0	0	0	0	0	0	0	LS Allocation				
2	**Counter 1**															
	0	0	0	0	0	0	0	CType	G/P Mode				Input Config			
3	**Counter 1: Minimum Count Value**															
4																
5	**Counter 1: Maximum Count Value**															
6																
7	**Counter 1: Minimum Rate Value**															
8																
9	**Counter 1: Maximum Rate Value**															
10																
11	**Counter 2**															
	0	0	0	0	0	0	0	CType	G/P Mode				Input Config			
12	**Counter 2: Minimum Count Value**															
13																
14	**Counter 2: Maximum Count Value**															
15																
16	**Counter 2: Minimum Rate Value**															
17																
18	**Counter 2: Maximum Rate Value**															
19																

Table 3.2 Counter Configuration Programming Block

Counter Configuration Programming Block (continued)

Block Notes

1) A counter must be disabled before it can be configured. Configuration data will not be accepted if the counter is enabled.

2) All data values are signed thirty-two bit integers (DINT's).

3) Programming configuration data resets all limit switch parameters to their default values.

Bit Descriptions

0.15: Transmit Bit. See the ***Transmit Bit*** section on page 21 for a description of this bit.

0.14: Echo Bit. When this bit is reset to zero, use the data in the programming block to program the ANH2. When this bit is set to one, ignore the remaining data and return the parameter values associated with this block to the host controller using the programming block's format. Bits 0.07-00 specify the programming block to return in the input data words.

0.09: Program Counter 2 Bit. If this bit is set, counter 2 is programmed using the data in words 11 through 19. If reset, the present configuration of counter 2 is left unchanged.

0.08: Program Counter 1 Bit. If this bit is set, counter 1 is programmed using the data in words 1 through 10. If reset, the present configuration of counter 1 is left unchanged.

0.07-00: Block Type Bits. Set to 0x01 to program or echo the Counter Configuration Programming Block.

1.04-00: LS Allocation. Valid range of 0 to 16. Sets number of limit switch setpoints allocated to Counter 1. Remaining setpoints are allocated to Counter 2.

2.08 or 11.08: Counter Type. "0" = Ring Counter. "1" = Linear Counter.

2.07-04 or 11.07-04: Gate/Preset Modes.

Bit 7	Bit 6	Bit 5	Bit 4	Gate/Preset Mode
0	0	0	0	Z input not used
0	0	0	1	Store/Continue
0	0	1	0	Store/Preset/Continue
0	0	1	1	Store/Hold/Resume
0	1	0	0	Store/Preset/Hold/Resume
0	1	0	1	Reserved
0	1	1	0	Reserved
0	1	1	1	Reserved
1	x	x	x	Reserved

Table 3.3 Gate/Preset Mode Bit Patterns

Counter Configuration Programming Block (continued)

Bit Descriptions (continued)

2:03-00 or 11:03-00: Input Modes.

Bit 3	Bit 2	Bit 1	Bit 0	Input Mode
0	0	0	0	Quadrature X4
0	0	0	1	Quadrature X2
0	0	1	0	Quadrature X1
0	0	1	1	Pulse / Internal Direction
0	1	0	0	Pulse / External Direction
0	1	0	1	Up / Down Pulses
0	1	1	0	Reserved
0	1	1	1	Reserved
1	x	x	x	Reserved

Table 3.4 Input Mode Bit Patterns

Data Words

Minimum Counter Value: Range of -2,147,483,648 to 2,147,483,646

Maximum Counter Value: Range of (Min Counter Value +1) to 2,147,483,647

Minimum Rate Value: -4,000,000 to 3,999,999

Maximum Rate Value: (Minimum Rate Value + 1) to 4,000,000

All data words are signed, thirty-two bit integers.

Limit Switch Programming Block

Word Number	Bit Number 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**Program Control Word**															
	TRMT	Echo	0	0	CLRBlk4	CLRBlk3	CLRBlk2	CLRBlk1	0	0	0	0001 = LS1 - LS4 0010 = LS5 - LS8 0100 = LS9 - LS12 1000 = LS13 - LS16				0
1	**Program LS and LS Type**															
	0	4thLSTimed	4thLSBase	Pgm4thLS	0	3rdLSTimed	3rdLSBase	Pgm3rdLS	0	2ndLSTimed	2ndLSBase	Pgm2ndLS	0	1stLSTimed	1stLSBase	Pgm1stLS
2 3	**1st Limit Switch Start Value (LS 1, 5, 9, or 13)**															
4 5	**1st Limit Switch Stop/Time Value (LS 1, 5, 9, or 13)**															
6 7	**2nd Limit Switch Start Value (LS 2, 6,10, or 14)**															
8 9	**2nd Limit Switch Stop/Time Value (LS 2, 6,10, or 14)**															
10 11	**3rd Limit Switch Start Value (LS 3, 7,11, or 15)**															
12 13	**3rd Limit Switch Stop/Time Value (LS 3, 7,11, or 15)**															
14 15	**4th Limit Switch Start Value (LS 4, 8,12, or 16)**															
16 17	**4th Limit Switch Stop/Time Value (LS 4, 8,12, or 16)**															
18	2nd Limit Switch Output Enable								1st Limit Switch Output Enable							
19	4th Limit Switch Output Enable								3rd Limit Switch Output Enable							

Table 3.5 LS Programming Blocks

Block Notes

1) The counter can be enabled and/or running when using this block. Limit switch programming data will also be accepted if the counter is disabled.

2) All data values are signed thirty-two bit integers (DINT's).

3) Programming configuration data resets all limit switch parameters to their default values.

Limit Switch Programming Block (continued)

Bit Descriptions

0.15: Transmit Bit See the ***Transmit Bit*** section on page 21 for a description of this bit.

0.14: Echo Bit. When this bit is reset, use the data in the programming block to program the ANH2. When this bit is set, ignore the remaining data and return the parameter values associated with this block to the host controller using the programming block's format. Bits 0.07-00 specify the programming block to return in the input data words.

0.11: Clear Block 4. When this bit is set, Limit Switches 13 - 16 are cleared. This occurs regardless of the programming block number being written to the ANH2. Clearing occurs before acting on any programming data that may be written to these limits as part of the programming block.

0.10: Clear Block 3. When this bit is set, Limit Switches 9 - 12 are cleared. This occurs regardless of the programming block number being written to the ANH2. Clearing occurs before acting on any programming data that may be written to these limits as part of the programming block.

0.09: Clear Block 2. When this bit is set, Limit Switches 5 - 8 are cleared. This occurs regardless of the programming block number being written to the ANH2. Clearing occurs before acting on any programming data that may be written to these limits as part of the programming block.

0.08: Clear Block 1. When this bit is set, Limit Switches 1 - 4 are cleared. This occurs regardless of the programming block number being written to the ANH2. Clearing occurs before acting on any programming data that may be written to these limits as part of the programming block.

0.07-00: Block Type Bits. Set as follows to program or echo the correct LS Programming Block.

Block Value (hex)	Programmed LS pairs
0x02	Program LS Setpoint pairs 00 - 03
0x04	Program LS Setpoint pairs 04 - 07
0x08	Program LS Setpoint pairs 08 - 11
0x10	Program LS Setpoint pairs 12 - 15

Table 3.6 LS Programming Bit Patterns

1.00: Program First LS Bit. Set this bit to program the first limit switch associated with this block (LS0, 4, 8 or 12) with the data in bits 1.01,02 and words 2 through 5.

1.01: First LS Base Bit. "0" = Count based limit switch. "1" = Rate based limit switch. Only acted upon when Program First LS Bit is set.

1.02: First LS Timed Bit. "0" = Normal limit switch. "1" = Timed limit switch. Only acted upon when Program First LS Bit is set.

1.04: Program Second LS Bit. Set this bit to program the second limit switch associated with this block (LS1, 5, 9 or 13) with the data in bits 1.05,06 and words 6 through 9.

1.05: Second LS Base Bit. "0" = Count based limit switch. "1" = Rate based limit switch. Only acted upon when Program Second LS Bit is set.

1.06: Second LS Timed Bit. "0" = Normal limit switch. "1" = Timed limit switch. Only acted upon when Program Second LS Bit is set.

1.08: Program Third LS Bit. Set this bit to program the first limit switch associated with this block (LS2, 6, 10 or 14) with the data in bits 1.09,10 and words 10 through 13.

1.09: Third LS Base Bit. "0" = Count based limit switch. "1" = Rate based limit switch. Only acted upon when Program Third LS Bit is set.

Limit Switch Programming Block (continued)

Bit Descriptions (continued)

1.10: Third LS Timed Bit. "0" = Normal limit switch. "1" = Timed limit switch. Only acted upon when Program Third LS Bit is set.

1.12: Program Fourth LS Bit. Set this bit to program the first limit switch associated with this block (LS3, 7, 11 or 15) with the data in bits 1.13,14 and words 14 through 17.

1.13: Fourth LS Base Bit. "0" = Count based limit switch. "1" = Rate based limit switch. Only acted upon when Program Fourth LS Bit is set.

1.14: Fourth LS Timed Bit. "0" = Normal limit switch. "1" = Timed limit switch. Only acted upon when Program Fourth LS Bit is set.

Limit Switch Start Value: The first limit switch setpoint. If the limit switch is a timed output, this setpoint sets the turn on point for the limit. This value is only acted upon when corresponding Program LS Bit is set.

Limit Switch Stop/Time Value: The second limit switch setpoint. If the limit switch is a timed output this setpoint sets the time in milliseconds that the limit is active. This value is only acted upon when corresponding Program LS Bit is set.

18:07-00: 1st LS Output Enable. Set the appropriate bit to associate the first setpoint pair programmed with this block with the output. (Bit 0 = Real Output 1, Bit 7 = Virtual Output 4). The final state of the output is the logical OR of all associated setpoint pairs.

18:15-08: 2nd LS Output Enable. Set the appropriate bit to associate the second setpoint pair programmed with this block with the output. (Bit 8 = Real Output 1, Bit 15 = Virtual Output 4). The final state of the output is the logical OR of all associated setpoint pairs.

19:07-00: 3rd LS Output Enable. Set the appropriate bit to associate the third setpoint pair programmed with this block with the output. (Bit 0 = Real Output 1, Bit 7 = Virtual Output 4). The final state of the output is the logical OR of all associated setpoint pairs.

19:15-08: 4th LS Output Enable. Set the appropriate bit to associate the fourth setpoint pair programmed with this block with the output. (Bit 8 = Real Output 1, Bit 15 = Virtual Output 4). The final state of the output is the logical OR of all associated setpoint pairs.

Save To Flash Programming Block

When the ANH2 accepts the Save To Flash block, it attempts to save all parameter values to Flash memory. The ACK bit is not set until the save is complete. In addition to the ACK bit (I0:15), the ANH2 will set the SvFlash bit (I0:10) to indicate that a save was attempted. The PgmErr bit (I0:11) is reset by the ANH2 on a successful write or set on a save to Flash error.

	Bit Number															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Program Control Word															
0	TRMT	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Words 1 - 19: Reserved, Must equal zero															

Table 3.7 Save to Flash Programming Blocks

Block Notes

1) The counters must be disabled when using this block.

2) The Acknowledge bit (ACK) in the network input data is not set until the save is complete. The ANH2 will also set the Save to Flash (SvFlash) bit if the save was successful or the Programming Error (PgmErr) bit if there was an error while saving the parameters. See ***Bit Descriptions*** on page 34 for additional information on these bits.

Bit Descriptions

0.15: Transmit Bit See the ***Transmit Bit*** section on page 21 for a description of this bit.

0.07-00: Block Type Bits. Set to 0x40 to save parameter values to Flash.

Restore Factory Defaults Programming Block

When the ANH2 accepts the Restore Factory Defaults block it attempts to restore all parameters to factory default values.

	Bit Number															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Program Control Word															
0	TRMT	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0
	Words 1 - 19: Reserved, Must equal zero															

Table 3.8 Save to Flash Programming Blocks

Block Notes

1) The counters must be disabled when using this block.

Bit Descriptions

0.15: Transmit Bit See the ***Transmit Bit*** section on page 21 for a description of this bit.

0.13: Restore Bit. This bit must be set to “1” when issuing the Restore Factory Default Settings block.

0.07-00: Block Type Bits. Must be set to 0x40.

Counter Control Block

The Counter Control Block controls the counter during normal operation. This block does not use the Transmit bit. Bit states and transitions are acted upon as soon as they occur. Each counter has a control bit that allows a value of zero to be written to the control word without changing Count Direction or Counter Enable states.

Word Number	Bit Number 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Program Control Word															
	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	Counter 1 Control Word															
	0	0	0	0	0	Cap-Ack	0	Preset1	Ctrl1	0	0	0	0	0	DirCtrl	Cntr1En
2	Counter 1 Preset Value															
3																
4	Counter 2 Control Word															
		0	0	0	0	Cap-Ack	0	Preset2	Ctrl2	0	0	0	0	0	DirCtr2	Cntr2En
5	Counter 2 Preset Value															
6																
7	Limit Switch Enable (1 enables LS setpoint pair)															
8	Force OFF Mask (1 turns output off)								Force ON Mask (1 turns output on)							
9	Reserved															
10	Reserved															
11	Reserved															
12	Reserved															
13	Reserved															
14	Reserved															
15	Reserved															
16	Reserved															
17	Reserved															
18	Reserved															
19	Reserved															

Table 3.9 Counter Control Block

Counter Control Block (continued)

Bit Descriptions

0.07-00: Block Type Bits. Set to 0x80 for the Counter Control Block. Note that the Transmit bit is not used with the Counter Control Block. This block is always acted upon immediately. Also note that the echo bit is not available with this block.

1.10: Capture 1 Acknowledge. Transition this bit to acknowledge that the new captured value has been processed by the host controller. If a capture event occurs before the previous event is acknowledged, the ANH2 will set the Capture Missed bit and replace the previous value with the new one. See ***Capture Value Handshaking*** on page 35 for a full explanation on how these bits operate together.

1.08: Software Preset Counter 1. On a zero to one transition on this bit, counter 1 will be preset to the thirty two bit Preset Value contained in words 2 and 3. Note that a software preset can occur even when the counter is disabled.

1.07: Control Counter 1 Bit. When set, the ANH2 will act upon the states of bits 1.01-00. When reset, the ANH2 ignores the state of bits 1.01-00. This bit allows the programmer to write a value of zero into this word without affecting the state of counter 1.

1.01: Counter 1 Count Direction. When the counter's input mode is set to "Pulse / Internal Direction", this bit sets the count direction for the counter. When this bit equals 0, pulses on the A input will increment the counter. When this bit equals 1, pulses on the A input will decrement the counter.

1.00: Counter 1 Enable. "0" = A and B inputs to counter 1 are disabled. Counter will not count, but can be preset from the backplane.

2 & 3: Counter 1 Preset Value: Thirty-two bit Preset Value for counter 1. Only acted upon when bit 1.08 makes a 0 → 1 transition or on a 0 → 1 transition on the Z input if the Gate Mode is set appropriately. A programming error results if this value is not within the following range:

- Min. Count Value <= Preset Value <= Max. Count Value

4.10: Capture 2 Acknowledge. Transition this bit to acknowledge that the new captured value has been processed by the host controller. If a capture event occurs before the previous event is acknowledged, the ANH2 will set the Capture Missed bit and replace the previous value with the new one. See ***Capture Value Handshaking*** on page 35 for a full explanation on how these bits operate together.

4.08: Software Preset Counter 2. On a zero to one transition on this bit, counter 2 will be preset to the thirty two bit Preset Value contained in words 5 and 6. Note that a software preset can occur even when the counter is disabled.

4.07: Control Counter 2 Bit. When set, the ANH2 will act upon the states of bits 4.02-00. When reset, the ANH2 ignores the state of bits 4.02-00. This bit allows the programmer to write a value of zero into this word without affecting the state of counter 1.

4.01: Counter 2 Count Direction. When the counter's input mode is set to "Pulse / Internal Direction", this bit sets the count direction for the counter. When this bit equals 0, pulses on the A input will increment the counter. When this bit equals 1, pulses on the A input will decrement the counter.

4.00: Counter 2 Enable. "0" = A and B inputs to counter 2 are disabled. Counter will not count, but can be preset from the backplane.

5 & 6: Counter 2 Preset Value: Thirty-two bit Preset Value for counter 2. Only acted upon when bit 4.08 makes a 0 → 1 transition or on a 0 → 1 transition on the Z input if the Gate Mode is set appropriately. A programming error results if this value is not within the following range:

- Min. Count Value <= Preset Value <= Max. Count Value

Counter Control Block (continued)

Bit Descriptions (continued)

7.15-00: Limit Switch Setpoint Pair Enable: When reset, the corresponding limit switch setpoint pair is disabled. the setpoint pair will not effect any associated output. When set, the corresponding setpoint pair is enabled. The setpoint pair will effect the on/off state of any associated output. Bit 0 corresponds to setpoint pair 1, bit 15 corresponds to setpoint pair 16.

8.15-08: Force OFF Bits. When reset, the state of the corresponding output is dependent on the state of the associated setpoint pairs and corresponding Force ON bit. When set, the corresponding output is off. Bit 8 corresponds to Real Output 1, bit 15 corresponds to Virtual Output 4.

8.07-00: Force ON Bits. When reset, the state of the corresponding output is dependent on the state of the associated setpoint pairs and corresponding Force OFF bit. When set, the corresponding output is on unless the corresponding Force OFF bit is also set. Bit 0 corresponds to Real Output 1, bit 7 corresponds to Virtual Output 4.

Echo Data Format

The Echo bit (Output Word 0.08) controls what data is reported to the host controller in the network input data. The Counter Configuration and LS Programming Blocks can be written down to the ANH2 with the Echo (0.08) bit set. When this bit is set, the ANH2 ignores the remaining data in the block and returns the present parameter values in the programming block's format. The Echo bit is returned as bit 8 of input word 0.

Echo Bit State (I0.8)	Description
0	Default Input Data (Table 4.1) is written to the host
1	Format of input data mirrors the format of programming block specified by Output Word 0, bits 07 - 00. Counter Configuration block format is table 3.2 on page 22. LS Programming Block format is table 3.5 on page 25 The data transferred is the present parameter values programmed with the specified block.

Table 3.10 Echo Bit States

Notes

Default Data Format

Word Number	Bit Number 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Module Status															
	ACK	Echo	MFlt	FOpen	Default	PgmErr	SvFlash	Heartbeat	Block Type 0x80 for block type shown							
1	Counter 1 Status															
	0	0	0	0	Cap-Miss	Cap-Ava	/PSet	ROvF	RUdF	COvF	CUdF	0	0	0	Counter State	
2	Counter 1: Count Value															
3																
4	Counter 1: Rate Value (counts /sec)															
5																
6	Counter 1: Captured Value															
7																
8	Counter 2 Status															
	0	0	0	0	Cap-Miss	Cap-Ava	/PSet	ROvF	RUdF	COvF	CUdF	0	0	0	Counter State	
9	Counter 2: Count Value															
10																
11	Counter 2: Rate Value (counts /sec)															
12																
13	Counter 2: Captured Value															
14																
15	Output Status															
	0	0	0	0	0	0	0	0	V4	V3	V2	V1	R4	R3	R2	R1
16	LS Setpoint Pair Enable States (1 = setpoint pair enabled)															
17	Force OFF Mask State								Force ON Mask State							
18	0	0	0	0	0	0	0	0	Error Codes							
19	0000h															

Table 4.1 Default Input Data Format

Default Data Format (continued)

Bit Descriptions

0.15 - ACK: Acknowledge Bit.

0.14 - Echo: Set when the data in the remaining words shows last valid parameter values instead of counter data. Bits 0.07-00 show which programming block is shown in the remaining words. See *Echo Data Format* on page 31 for more information.

0.13 - MFlt: Module Fault. Set when the module fails its power on self test.

0.12 - FOpen: Fuse Open. Set when output fuse is in its open (non-conducting) state.

0.11 - Default: Module is using factory default parameter values. Set on power up or hardware reset if factory default values are restored from Flash memory.

0.10 - PgmErr: Programming Error. Only valid while the ACK bit is set, this bit is set when the last programming block contains data errors. Error codes are contained in the Error Codes byte (18.07-00).

0.09 - Save To Flash Complete: Only valid while ACK Bit is set, this bit is set when a Save to Flash command has been completed. Error Codes byte = 0x00 when save is successful. Error Codes byte = 0x60 when there is an error saving to Flash.

0.08 - Heartbeat: This bit changes state every 50 milliseconds. It is not available when echoing back programming data. Data is being echoed back when the Echo bit (0.14) is set.

1.11 or 8.11 - Capture(1,2) Missed: Set when one or more Captured Values were missed by the host. This bit is only updated when the corresponding Capture Available (Cap-Ava) bit transitions. This bit can only be reset by cycling power to the module or programming new configuration data.

1.10 or 8.10 - Capture(1,2) Available: Capture Available: This bit transitions when a new captured value is available. Only the latest value is reported. If multiple capture events occur between host controller updates, these values are lost and the corresponding Capture Missed bit is also set. The host controller must transition the corresponding Capture Acknowledge bit to acknowledge that the new captured value has been processed. See ***Capture Value Handshaking*** on page 35 for a full explanation on how these bits operate together.

1.09 or 8.09 - /Preset: Counter Not Preset. Set when counter has not been preset since power up or last hardware reset. Once the counter is preset from the network or the Z input, this bit is reset.

1.08 or 8.08 - ROvF: Rate Overflow. Rate value greater than programmed Maximum Rate Value.

1.07 or 8.07 - RUdF: Rate Underflow. Rate value less than programmed Minimum Rate Value.

1.06 or 8.06 - COvF: Counter Overflow. Counter programmed as linear counter and count value is greater than the programmed Maximum Count Value parameter.

1.05 or 8.05 - CUdF: Counter Underflow. Counter programmed as linear counter and count value is less than the programmed Maximum Count Value parameter.

1.01-00 or 8.01-00: Counter State. 00 = Stop State. 01 = Run State. 10 = Hold State. 11 = Reserved

Words 2&3 or 9&10: Present Count Value as a 32 bit signed integer.

Words 4&5 or 11&12: Present Rate Value as a 32 bit signed integer. Resolution of 1 Hz.

Words 6&7 or 13&14: Captured Count Value as a 32 bit signed integer.

15.07-00: Output States. State of the outputs. bits 7-4 are the virtual outputs, 3-0 are the real outputs. Bit 15.00 corresponds to Real Output 1.

Default Data Format (continued)

Bit Descriptions (continued)

Word 16: LS Setpoint Pair Enabled States. Each bit reports back the enabled state of the corresponding setpoint pair. This word mirrors word 7 of the Counter Control Block. "1" = LS is enabled. Bit 0 corresponds to LS0.

17.15-08: Force OFF Mask state. This byte mirrors the upper byte of word 8 in the Counter Control Block. "1" = Output is forced OFF. Bit 8 corresponds to real output 1.

17.07-00: Force ON Mask state. This byte mirrors the lower byte of word 8 in the Counter Control Block. "1" = Output is forced ON if corresponding bit in Force OFF Mask equals "0". Bit 0 corresponds to real output 1.

18.07-00: Error Codes. See ***Error Codes*** starting on page 37 for a list of all available error codes.

Capture Value Handshaking

The ANH2 uses three bits per counter to perform the following tasks:

- To signal the host controller that a new captured value is available
- To accept a signal from the host controller that the captured value has been read
- To signal the host controller when a captured value has been missed and overwritten with new data.

The three bits per counter used to perform these tasks are:

- **Capture(1,2) Available:** *Input word 1, bit 10 for counter 1 and Input word 8, bit 10 for counter 2.* This bit *transitions*, (either 0 → 1 or 1 → 0) when a new captured value is available from the ANH2.
- **Capture(1,2) Acknowledge:** *Output word 1, bit 10 for counter 1 and Output word 4, bit 10 for counter 2 when using the Counter Control Block.* The host must *transition* this bit (either 0 → 1 or 1 → 0) to signal to the ANH2 that the host has processed the latest captured value and is ready to accept the next one.
- **Capture(1,2) Missed:** *Input word 1, bit 11 for counter 1 and Input word 8, bit 11 for counter 2.* This bit is set to "1" if the host controller did not respond to a change in state of the Capture Acknowledge bit before a new value is captured. The ANH2 will update its captured value registers to the new value whenever a capture occurs. This bit remains set until the counter's configuration is reprogrammed or power is cycled to the module.

Capture Value Handshaking (continued)

The figure below shows how these bits work together.

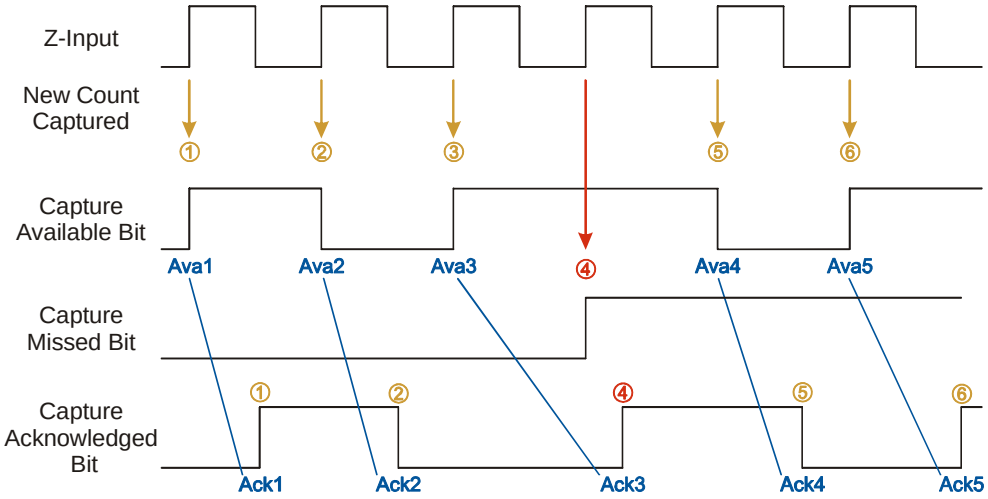


Figure 4.1 Capture Value Handshaking

- A new value is captured on every positive transition on the Z input.
- The ANH2 transitions the Capture Available bit to inform the host controller that a new captured value is available.
- The first two capture events are acknowledged by the host controller before the next capture event occurs.
- Capture event (4) occurs before the third event is acknowledged. The Capture Missed Bit turns on at this point and the Captured Value registers from the ANH2 are updated to the value captured at (4). The value captured at (3) is lost.
- The Captured Acknowledged bit Ack3 acknowledges the value captured at event (4).
- At capture event (5), the ANH2 transitions the Capture Available bit to inform the host controller that a new captured value is available. (The value for capture event (5) is reported to the host.) The Capture Missed bit remains on until a Configuration Programming Block is written to the ANH2 or poser is cycled to the module.
- Capture event (5) is acknowledged before capture event (6) occurs.

Figure 4.2 shows one method of buffering captured values and responding to the Capture Available bit in your program.

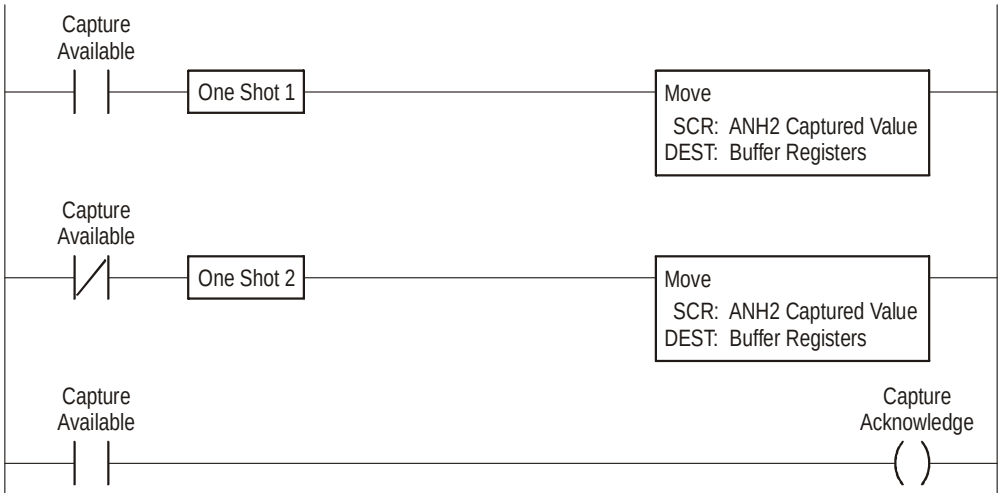


Figure 4.2 Buffering Captured Values

CHAPTER 5
ERROR CODES

Error Coder Format

- Bit 7: Always equals zero
- Bits 6,5:
  - 00 = General or Control Error.
  - 01 = Config block error.
  - 10 = LS Programming Error.
  - 11 = Flash Error
- Bit 4:
  - 0 = General or Counter 1 error.
  - 1 = Counter 2 error
- Bits 3-0: Error value within blocks define by bits 6&5

Available Error Codes

0x00: No Errors

0x01: Reserved bits or words in the Network Output Data Block were not equal to zero.

0x02: More than one bit in Block Type Bits (0.07-00) is set, or they equal 0x00

0x03: Config. Block - Echo (0.14), Pgm2 (1.09) and Pgm1 (1.08) bits all equal zero

0x04: LS Block - Echo (0.14), all ClrBlk (0.11-08) and all Pgm'n'LS (1.12,08,04,00) bits equal zero.

0x05: Counter 1 Control Error. Reserved bits were set or the direction bit was set and not in pulse/internal direction mode.

0x0F: Counter 1 Preset Value Error. Preset Value 1 outside its valid range when Preset1 (1.07) or Z input is active. This value is always checked, even if the channel is in its disabled state.

0x15: Counter 2 Control Error. Reserved bits were set or the direction bit was set and not in pulse/internal direction mode.

0x1F: Counter 2 Preset Value Error. Preset Value 2 outside its valid range when Preset2 (4.07) or Z input is active. This value is always checked, even if the channel is in its disabled state.

0x20: LS Allocation outside it's range of 0 to 16.

0x21: Counter 1: Invalid Gate/Preset Mode (reserved pattern)

0x22: Counter 1: Invalid Input Mode (reserved pattern)

0x23: Counter 1: Max. Count <= Min. Count

0x24: Counter 1: (Max. Rate <= Min. Rate) or (Max.Rate > 4,000,000) or (Min. Rate < -4,000,000)

0x25: Counter 1: Programming Error:

- Attempted to program configuration values while the channel was not in its disabled state.
- You issued a Save to Flash command while the counters are not both disabled.
- You attempted to echo back Limit Switch programming data while the channel was not in its disabled state.

0x31: Counter 2: Invalid Gate/Preset Mode (reserved pattern)

0x32: Counter 2: Invalid Input Mode (reserved pattern)

0x33: Counter 2: Max. Count <= Min. Count

0x34: Counter 2: (Max. Rate <= Min. Rate) or (Max.Rate > 4,000,000) or (Min. Rate < -4,000,000)

0x35: Counter 2: Programming Error:

- Attempted to program configuration values while the channel was not in its disabled state.
- You issued a Save to Flash command while the counters are not both disabled.
- You attempted to echo back Limit Switch programming data while the channel was not in its disabled state.

Available Error Codes (continued)

0x40: Start Value 1 outside its range. (Range set by min/max count or rate values)
0x41: Stop Value 1 outside its range. (Range set by min/max count or rate values or {1 to 32,767} if timed.)
0x42: Start Value 1 = Stop Value 1, including when both equal zero.
0x43: Start Value 2 outside its range. (Range set by min/max count or rate values)
0x44: Stop Value 2 outside its range. (Range set by min/max count or rate values or {1 to 32,767} if timed.)
0x45: Start Value 2 = Stop Value 2, including when both equal zero.
0x46: Start Value 3 outside its range. (Range set by min/max count or rate values)
0x47: Stop Value 3 outside its range. (Range set by min/max count or rate values or {1 to 32,767} if timed.)
0x48: Start Value 3 = Stop Value 3, including when both equal zero.
0x49: Start Value 4 outside its range. (Range set by min/max count or rate values)
0x4A: Stop Value 4 outside its range. (Range set by min/max count or rate values or {1 to 32,767} if timed.)
0x4B: Start Value 4 = Stop Value 4, including when both equal zero.
0x60: Save to Flash Error. Cycle power to the ANH2 to attempt to clear the error.

CHAPTER 6
DEFAULT PARAMETER VALUES

Counters

Counter 1 and 2 have identical configurations.

- Counter Type: Ring Counter (0x0 value)
- G/P Mode: Z input not used (0x0 value)
- Input Mode: Pulse/Internal (0x3 value. Allows counting with just about anything attached.)
- Minimum Counter Value: -2,147,483,648
- Maximum Counter Value: 2,147,483,647
- Minimum Rate Value: -4,000,000
- Maximum Rate Value: 4,000,000

Limit Switches

All limit switch outputs are disabled.

- LS Allocation: 16. (All limits assigned to counter 1.)
- LS Base: Count based
- LS Type: Normal Limit Switch, not Timed.
- LS On/Off Setpoints: All equal to zero.
- Limit Switch Output Enable: 0x00

Masks

- Limit Switch Setpoint Enable: 0x0000
- Force OFF Mask: 0x00
- Force ON Mask: 0x00

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